Applicant points out that UK Application No. 9814014.8 is the application to which priority is claimed in this application as indicated in the Declaration that was filed on August 10, 1999.

A copy of the Supplemental Response including a copy of the cover page, the request for grant, and the first page of claims of the certified priority document is enclosed as evidence of Applicant's submission of the Supplemental Response. Also enclosed is a copy of the return receipt postcard that was submitted along with the Supplement Response evidencing receipt of the Supplemental Response and the enclosed certified priority document by the United States Patent and Trademark Office Mailroom on March 5, 2002.

In view of the fact that a certified copy of UK Application No. 9814014.8 has been submitted in this application, as evidenced by the enclosed documents, Applicant respectfully requests acknowledgement of receipt of same.

The Office Action rejected claims 1-7 under 35 U.S.C. §102(e) as being anticipated by Aleksic (U.S. Patent Number 5,995,736). Applicant respectfully traverses this rejection.

Aleksic is directed to a method and system for automatically modeling registers for integrated circuit design (col. 1, lines 6-9). As illustrated in Figure 2 of Aleksic, a system 32 for automatically modeling registers includes a common register description source data 34, which is description data representing grouped register data in the form of a text file. This text file serves as the source for automatically generating hardware design simulation code and behavioral model code (col. 5, lines 9-18). System 32 also includes a model register generator which accesses the register description source data 34 to generate the behavioral model code, the hardware simulation code, the application interface layer code 42, automatic register tests 44, integrated circuit documentation 46, software header information 48, and connection templates 49 (col. 5, lines 19-29). The behavioral model code 40 and the hardware simulation code 38 make up a coded register layer which defines characteristics of each register block. The hardware design simulation code 38 and the behavioral model register code 40 is based on the register description source data 34, thus the register layer is also based on the register description source data 34 (col. 5, lines 43-54). Hence, Aleksic discloses that the behavioral model register code and the hardware design simulation code are both generated from the register description source data 34. Indeed, Aleksic teaches that it is important that the behavioral model register code and the hardware design simulation code be generated from "a common input of source to insure that any changes are automatically included in each phase of design" (col. 3, lines 53-58).

Aleksic further discloses that the behavioral model code and the hardware simulation code are tested in parallel. For example, in col. 7, lines 61 thorough col. 8, line 7, Aleksic discloses that once the behavioral model register code 40 and the hardware design simulation code are generated, the system complies the code in a form suitable for testing. The automatic register generator 36 pulls register file data from the register specification source 34 to populate test code templates for testing both the behavioral model register code 40 and the hardware design simulation code 38. The system then runs the test on the behavioral model register code and the hardware design code using the register test code 44.

Claim 1 is directed to a method of simulating an application specific processor (ASP). The method comprises acts of defining a functional model in a high level language, generating for each peripheral an interface functions file and a test functions file, simulating in the high level language an application executable by the CPU and operations of the set of peripherals, outputting the state of the application and the state of the peripherals to a modeling file, converting the modeling file to a simulation language for simulating the ASP at circuit level, and simulating the ASP at circuit level.

Unlike the method of simulation disclosed by Aleksic, in which the behavioral model and the hardware model are generated and tested in parallel, claim 1 recites acts of outputting the state of the application and the state of the peripherals at the end of a predetermined simulation phase to a modeling file in the high level language and converting the modeling file in the high level language to a simulation language for simulating the ASP at the circuit level. Aleksic fails to disclose or suggest using state data output from testing of the functional model as input for the circuit level simulation. Indeed, Aleksic teaches away from Applicant's invention as recited in claim 1, in that Aleksic discloses generating and testing the behavioral model and the hardware simulation model in parallel (col. 7, line 61 - col. 8, line 7). Thus, claim 1 patentably distinguishes over Aleksic. Accordingly, it is respectfully requested that the rejection of claim 1 under 35 U.S.C. §102(e) be withdrawn.

Claims 2-5 depend from claim 1 and are patentable for at least the same reasons discussed above in connection with claim 1. Accordingly, it is respectfully requested that the rejection of claims 2-5 under 35 U.S.C. §102(e) be withdrawn.

Claim 6 is directed to a computer system for simulating an ASP. The computer system comprises first processor means including execution means for simulating a functional model in a high level language and output means for outputting the state of the functional model at the end

of a predetermined simulation phase. Claim 6 further comprises means for converting the function model, including its state at the end of the predetermined simulation phase, into a simulation language for simulating the ASP at circuit level and second processor means arranged to execute the simulation language to simulate the ASP at circuit level for a subsequent simulation phase. As discussed above in connection with claim 1 Aleksic fails to disclose or suggest means for simulating an ASP in which the state of the functional model at the end of a simulation phase is used to simulate the ASP at circuit level. Aleksic discloses generating and testing the behavioral model and the hardware simulation model in parallel. Thus, claim 6 patentably distinguishes over Aleksic. Accordingly it is respectfully requested that the rejection of claim 6 under 35 U.S.C. §102(e) be withdrawn.

Claim 7 is directed to a modeling file stored on a computer readable medium which comprises a first code portion holding a test functions file defining the communication attributes of a processor with a peripheral of an ASP to be simulated and including the state of the test functions file after a predetermined simulation phase and a second code portion holding an interface functions file which defines the communications attributes of the peripheral with the processor and the functional attributes of the peripheral and including the state of the interface functions file after a predetermined simulation wherein the code portions are within a circuit level simulation language and are executable by a computer in which the modeling file is loaded to simulate the ASP at the circuit level for subsequent simulation phase.

As discussed above, Aleksic discloses generating and testing the behavioral model and the hardware's emulation model in parallel. Aleksic fails to disclose or suggest using state of the simulation of the functional model to simulate the ASP at the circuit level in a subsequent simulation phase. Thus, claim 7 patentably distinguishes over Aleksic. Accordingly, it is respectfully requested that the rejection of claim 7 under 35 C.F.R. §102(e) be withdrawn.

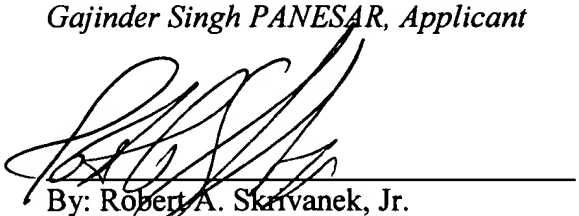
CONCLUSION

In view of the foregoing remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes after this response that the application is not in condition for allowance, the Examiner is requested to call Applicant's attorney at the number listed below to discuss any outstanding issues relating to allowability.

If this response is not considered timely filed, and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by the enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,

Gajinder Singh PANESAR, Applicant



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